DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claim 2 have been considered but are moot in view of the new ground(s) of rejection

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2, 14, 15, 17, 21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitani et al. (USPN 6,191,463 B1) in view of Wristers et al. (USPN 5,674,788).

4. In reference to claim 2, Mitani et al. (USPN 6,191,463 B1, hereinafter referred to as the "Mitani" reference) discloses a similar device. In claim 9 of Mitani (column 44, lines 9-19), a substrate is described with a gate electrode over a gate insulator. The gate insulator is composed of a combination of silicon, oxygen, nitrogen, and fluorine (a halogen element).

Mitani does not disclose the exact nitrogen atom concentration of the applicant (more than 1×10^{20} cm^{-3}). However it is known in the semiconductor art that having a nitrogen atom concentration of this quantity in a gate insulator has the benefit of preventing the penetration of boron atoms into the gate insulator. This is disclosed by Wristers et al. (USPN 5,674,788,

hereinafter referred to as the "Wristers" reference) in column 8, lines 2-6. Therefore it would be obvious to utilize a gate insulator having a nitrogen concentration greater than 1 x 10^{20} atoms/cm^2 in the device of Mitani so as to attain the advantage of preventing boron penetration into the gate insulator.

5. Regarding claim 14, the device of Mitani constructed in view of Wristers meets the claim. In claim 9 of Mitani, the fluorine concentration of the gate insulator is 1 x 10^{20} atoms/cm^3 to 1 x 10^{21} atoms/cm^3. This meets the limitation where the fluorine concentration is more than 1 x 10^{19} atoms/cm^3.

6. Regarding claims 15, 17, 21 and 23, both Mitani and Wristers utilize boron doped polysilicon gates. In the device of Mitani constructed in view of Wristers, boron diffusion into the substrate is prevented by a gate insulator having a nitrogen concentration greater than 1 x 10^{20} atoms/cm^2.

7. Claims 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitani et al. (USPN 6,191,463 B1) in view of Wristers et al. (USPN 5,674,788) and further in view of Gardner et al. (5,851,888).

8. Regarding claims 18 and 20, neither Mitani nor Wristers discloses the exact thickness. However the use of thin gate dielectrics is well known in the art. Gardner et al. (USPN 5,851,888, hereinafter referred to as the "Gardner" reference) discloses a 3 nm nitrided gate insulator (claim 1). Such thin gate dielectrics are used for the advantage of reducing short channel effects (column 1, lines 30-32). It would therefore be obvious to construct the nitrided gate insulator of the device of Mitani constructed in view of Wristers with a thickness of 3 nm; which is between 0.5-5 nm.

Allowable Subject Matter

9. Claims 13, 16, 19, and 22 are allowed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). In particular, amended claim 2 necessitated the new grounds of rejection.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

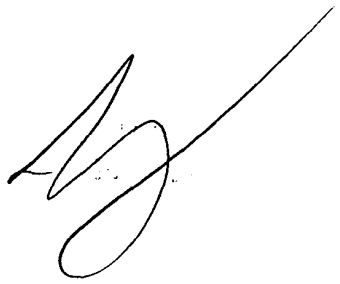
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ
March 11, 2002



INSULATED GATE TRANSISTOR AND PROCESS FOR FABRICATING THE SAME

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device equipped with a gate insulator in an insulated gate transistor, as well as to a process for fabricating the semiconductor device.

In recent years, because of necessities for the suppression of variations in threshold voltages of transistors as well as for the suppression of the short-channel effect, there have been developed CMOS having a dual-gate structure using surface-channel type transistors that employ a gate containing N-type impurities for NMOS and a gate containing P-type impurities for PMOS. This has been reported, for example, in International Electron Devices Meeting 1996, pp. 555 - 558.

However, in an attempt to form the dual-gate structured CMOS with surface-channel type transistors, there is a problem as follows. That is, when P-type doped polysilicon is used as a gate electrode, boron in the gate electrode penetrates through the gate oxide in heat treatment process for activation of impurities, reaching

substrate silicon and making the threshold voltage of transistors largely changed.

For this reason, it has been reported in International Electron Devices Meeting 1990, pp. 429 - 432 that the penetration of boron can be suppressed by using nitride oxide as the gate insulator.

It has also been reported in IEEE Electron Device Lett. 10,141 (1989) that when polysilicon film containing no boron is used as the gate electrode, transistor characteristics and reliability are improved by introducing fluorine to the gate insulator.

However, it is reported in Symposium on VLSI technology, 1990, pp. 131 - 132 that using nitrided oxide film as the gate insulator would cause the mobility of transistors to be reduced, as compared with using oxide film.

In another aspect, as the surface-channel type P-type transistor, those in which polysilicon film containing boron as the P-type dopant is used as the gate electrode are the current mainstream. With such gate insulator given by silicon oxide and with fluorine contained in the gate electrode, fluorine accelerates the diffusion of boron, making it more likely that boron reaches the substrate silicon. This leads to a problem that the threshold voltage of the P-type transistor becomes more liable to vary.

In a further aspect, whereas gate insulated type transistors having a floating electrode and a control gate are used as nonvolatile memory, there has been a growing demand for transistors having a thinner gate insulator along with the scaling-down of devices. However, because a high electric field is applied to the gate insulator used in nonvolatile memory, the gate insulator would progressively deteriorate as its thickness decreases, which would cause a problem that the leak current increases. This deterioration begins to appear noticeably when the oxide film thickness becomes thinner than 10 nm, and tends to exponentially increase as the film thickness decreases.

This being the case, as a result of the inventor's keen studies with a view to preventing boron from penetrating and diffusing into the substrate, and to avoiding the reduction of the mobility of the transistors, the present invention has been achieved.

In order to achieve the afore mentioned object, there is provided an insulated gate transistor having a gate electrode on a substrate with a gate insulator interposed therebetween, wherein the gate insulator composed of silicon and oxygen contains both nitrogen atoms and halogen atoms.

Because nitrogen and a halogen element are contained in the gate insulator, interface deterioration due